DOCUMENT REVISION STATUS

REV	EO/ECN	CHECK	DATE	ENGR	DATE	REV	EO/ECN	CHECK	DATE	ENGR	DATE
A	14999	H. Bloom	10/6/80	N. Massa	10/7/80						
B	15143	G.J.	12/4/80	N. Massa	2/23/81						

SHEET REVISION STATUS

SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV	SHEET	REV
1	B	16	B												
2	B	17	B												
3	B	18	B												
4	B	19	B												
5	B	20	B												
6	B	21	B												
7	B	22	B												
8	B	23	B												
9	B	24	B												
10	B	25	B												
11	B	26	B												
12	B	27	B												
13	B														
14	B														
15	B														

ISB 3110 8085 BASED

PROCESSOR CARD

INTERSIL
75 HAMMERWOOD AVENUE
SUNNYVALE, CA. 94086

TITLE: SPEC-ISB 3110

NEXT ASSEMBLY

SYSTEM: STD BUS

DOCUMENT NO.: 22-00003

SHEET 1

TABLE OF CONTENTS

1.0 FEATURES:

- Fully buffered signals for system expandability.
- Up to 8K Bytes EPROM capacity, in 2 or 4K Bytes increments (two EPROM sockets).
- Up to 4K Bytes Static RAM capacity, in 1K increments.
- Jumper selectable (2716 or 2732 EPROMS).
- Full Memory decoding capability to map on board EPROM/$\overline{\text{RAM}}$ anywhere in 64K Bytes address field in 4K increments.
- Full Bus arbitration circuitry to arbitrate between: On board memory access/Off board memory access, on board I/O operation/ Off board I/O operation.
- 3 independent timer/counter channels with interrupting capability and daisy chain priority interrupt arbitration for all three channels.
- Programmable power on restart to jump anywhere in the address field.
- Power on reset/pushbutton reset input.
- 6.144 or 8 MHz crystal oscillator frequency available.
- Jumper selectable external clock input for 8085 processor or any of the timer/counters.
- 3 State Address, Data and Control Bus.
- Single +5V supply.

2.0 DESCRIPTION:

The Intersil ISB 3110 is an 8085 based STD Bus compatible Processor Module on a 6.5" x 4.48" card.

The card contains space for 4K bytes of Static RAM in 1K increments utilizing the popular 2114 (1K x 4) Static RAMS. It also contains two socket locations for EPROMS; either 2716 (2K x 8) or 2732 (4K x 8) can be selected through the jumper strap. Three independent timer/counter channels with interrupting capability utilizing RST 7.5, 6.5, 5.5 by connecting them to out 2, 1, Ø of timer/counter and daisy chain priority arbitration are also provided. Fast (8MHZ crystal frequency) or slow (6.144 MHZ crystal frequency) are available. Other features include power on reset/push button reset inputs, jumper selectable external clock input for processor or any of the timer/counter channels, fully buffered, 3 state Address/Data/Control signals to the bus.

The memory mapping for on board RAMS and EPROMS are jumper selectable and can be mapped in 4K blocks anywhere on the 64K memory field in 4K increments. On board, RAMS and EPROMS can also be totally bypassed and removed from the board.

Bus arbitration logic ensures proper arbitrations between the following operations:

On board memory vs. Off board memory.
On board I/O vs. Off board I/O.

The CPU on power on Restart can start at X'0000' or be programmed to jump to any location within the address field. If the later is chosen, 3 bytes of the first EPROM on the board is to be used to store the jump address. After reading the starting address, the circuitry disables the EPROM or maps it at other preassigned location other than X'0000'.

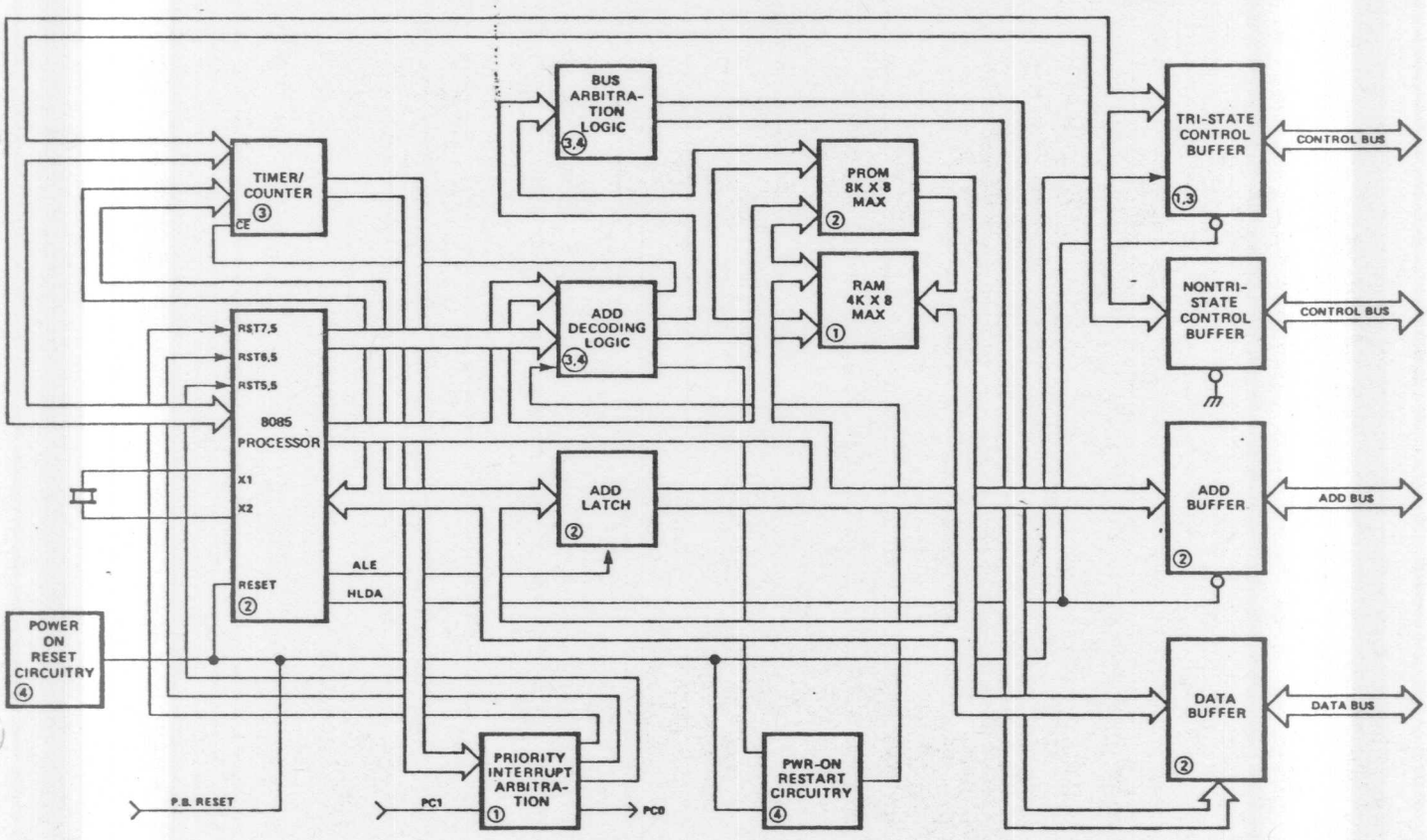

BUS ARBITRATION LOGIC
3,4
TIMER/ COUNTER
3
CE
PROM 8K X 8 MAX
2
RAM 4K X 8 MAX
1
ADD DECODING LOGIC
3,4
TRI-STATE CONTROL BUFFER
1,3
CONTROL BUS
NONTRI-STATE CONTROL BUFFER
CONTROL BUS
RST7,5
RST6,5
RST5,5
8085 PROCESSOR
X1
X2
RESET
2
ALE
HLDA
ADD LATCH
2
ADD BUFFER
2
ADD BUS
POWER ON RESET CIRCUITRY
4
DATA BUFFER
2
DATA BUS
PRIORITY INTERRUPT ARBITRATION
1
PC1
PC0
P.B. RESET
PWR-ON RESTART CIRCUITRY
4

FIG: 1

3.0 SPECIFICATIONS

3.1 Word Size

8 Bits Data Bus
Instruction: 8, 16, 24

3.2 Clock Period (T State):

327 or 250 ns

3.3 Memory Capacity:

On Board EPROMS up to 8K Bytes.
On Board RAMS up to 4K Bytes.
Off Board expansion - up to 64K Bytes, with user specified combination of RAM, ROM, EPROM.

3.4 Memory Mapping:

On board EPROMS: Jumper selectable 2716 (2K bytes) or 2732 (4K bytes).

Jumper selectable for any 4K boundary within 64K address field. If 2732 is used, two 4K EPROMS can be mapped completely independent from each other within 64K address field.

On board RAMS: Jumper selectable for any 4K boundary within 64K address field.

3.5 Memory speed required:

		Access Time for Fast Card	Access Time for Slow Card
EPROM:	2716 or 2732	400 ns max.	450 ns max.
RAM:	Dynamic or Static	400 ns max.	450 ns max.

3.6 I/O Addressing

On Board programmable Timer

PORT ADDRESS (HEX)	CHANNEL
7C	0
7D	1
7E	2
7F	-

3.7 I/O Capacity

Up to 256 can be decoded off board. The three port addresses, (7C, 7D, 7E, 7F) are used for On Board Timer/Counter and can not be used for any Off Board peripheral.

3.8 Interrupts

Multi level vector interrupt - interrupt request may originate from user specified I/O only. Timer counter channels interrupt CPU through RST 7.5, RST 6.5, RST 5.5 inputs.

3.9 Power Supply Requirement

+5V ± 5% at 1.5A max.

4.0 INTERFACE:

All address, data and command signals are TTL compatible.

5.0 MATING CONNECTOR:

See Table 1

6.0 CARD DIMENSIONS:

Length - 6.5 inches, 16.51 cm
Heigth - 4.48 inches, 11.38 cm
Thickness - .062 inches, .158 cm
Component Height Above Board - 0.338", 0.858 cm

7.0 ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0^{o} to $55^{o}C$
Storage Temperature: -40^{o} to $80^{o}C$
Relative Humidity: 0% to 90% without condensation

TABLE 1 - COMPATIBLE EDGE CONNECTORS

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR P/N
STD BUS	28/56	0.125 In.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW28 DO-111
STD BUS	28/56	0.125 In.	Wire Wrap	Viking Winchester	VH28/ICHD5 HW28 DO-111

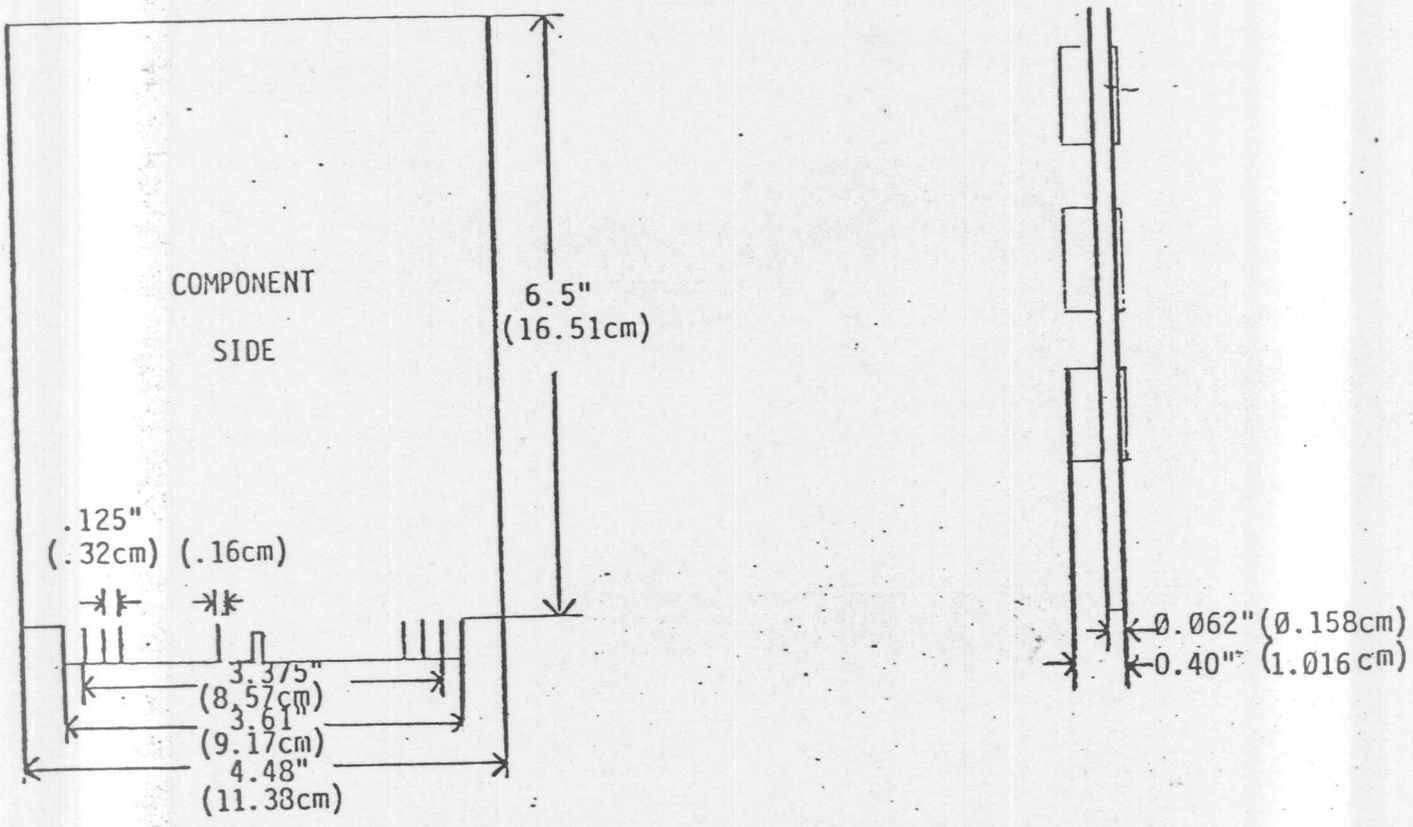


FIGURE 2 - STANDARD CARD OUTLINE

8.0 STD BUS ORGANIZATION AND FUNCTIONAL SPECIFICATIONS (WITH PIN DEFINITIONS)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1-6
Data Bus	Pins 7-14
Address Bus	Pins 15-30
Control Bus	Pins 31-52
Auxilliary Power Bus	Pins 53-56

TABLE 2 - STD BUS

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
POWER BUS	53	AUXGND	In	AUX Ground (Bussed)	54	AUXGND	In	AUX Ground (Bussed)
	55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX-V.	In	AUX Negative (-12 Volts DC)

*Low Level Active Indicator

8.1 Data and Address Signals

8.1.1 Data Bus - Pins 7-14

An 8-Bit bidirectional 3-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and interrupt Acknowledge ($\overline{INTAK}$).

The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers.

8.1.2 Address Bus - Pins 15-30

A 16-bit 3 state high-level active bus. The address will normally originate at the processor card. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller.

The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request (IORQ) control lines are used to distinguish between the two operations. The particular microprocessor used will determine the number of address lines and how they are used.

TABLE 3 ISB-3110 STD BUS SIGNAL FUNCTIONS (CONTINUED)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 0}}$	40	*Status Control Line 0* — Used in conjunction with $\overline{\text{STATUS 1}}$ to indicate the type of CPU cycle in progress.
$\overline{\text{BUSAK}}$	41	*BUS Acknowledge* — An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an Acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle.
$\overline{\text{BUSRQ}}$	42	*Bus Request* — An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed.
$\overline{\text{INTAK}}$	43	*Interrupt Acknowledge* — An active-low output line from the processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during $\overline{\text{INTAK}}$.
$\overline{\text{INTRQ}}$	44	*Interrupt Request* — An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping $\overline{\text{INTAK}}$.
$\overline{\text{WAITRQ}}$	45	*Wait Request* — An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus.
$\overline{\text{NMIRQ}}$	46	*Non-Maskable Interrupt* — An active-low processor card interrupt input line of highest priority.
$\overline{\text{SYSRESET}}$	47	*System Reset* — An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization.
$\overline{\text{PBRESET}}$	48	*Push Button Reset* — An active-low input line to the processor.
$\overline{\text{CLOCK}}$	49	*Clock From Processor* — A buffered processor clock signal used for system synchronization or as a general clock source.
$\overline{\text{CNTRL}}$	50	*Control* — An external clock input for special clock timing.
PCO	51	*Priority Chain Output (Output, active-high)* — This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	*Priority Chain In (Input, active-high)* — This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.

TABLE 3 ISB-3110 STD BUS SIGNAL FUNCTIONS

$\overline{WR}$	31	*Write to Memory or I/O* – A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device.
$\overline{RD}$	32	*Read from Memory or I/O* – A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS.
$\overline{IORQ}$	33	*I/O Address Select* – A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	34	*Memory Address Select* – A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations.
$\overline{IOEXP}$	35	*I/O Expansion* – An active-low control signal used to expand or enable I/O Port addressing.
$\overline{MEMEX}$	36	*Memory Expansion* – An active-low control signal used to expand or enable memory addressing.
$\overline{REFRESH}$	37	*Dynamic Memory Refresh* – a tri-state, active-low control line normally used to refresh dynamic memory. This signal is not generated on this processor card.
$\overline{MCSYNC}$	38	*Machine Cycle Sync* – A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle.
$\overline{STATUS\ 1}$	39	*Status Control Line 1* – Used in conjunction with $\overline{STATUS\ 0}$ to indicate the type of CPU cycle in progress.

TABLE 4 - LOGIC POWER

• +5V	PINS 1 & 2	+5 Logic Voltage (VCC) Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
• GND	PINS 3 & 4	Logic Ground Ground for logic power. Both pins are bussed together for current capacity.

9.0 BOARD OPTIONS & UTILIZATIONS:

9.1 Memory Mapping (FIG: 3 and 4)

RAMS and EPROMS residing on CPU card can be mapped in 4K blocks independently anywhere within 64K address field.

		PAD
$\overline{EN1}$	= First 4K blocks of EPROM	E3
$\overline{EN2}$	= Second 4K block of EPROM	E11
$\overline{CSR}$	= 4K block or RAM	E4

Each one of the above 4K blocks can be independently moved within 64K address field in 4K increments. The pad designating the starting address for each 4K boundaries are as follows:

PAD	DESIGNATED STARTING ADDRESS
E2	0000H
E13	1000H
E14	2000H
E15	3000H
E16	4000H
E17	5000H
E18	6000H
E19	7000H
E20	8000H
E21	9000H
E22	A000H
E23	B000H
E24	C000H
E25	D000H
E1	E000H
E26	F000H

By jumpering the appropriate pads. $\overline{EN1}$, $\overline{EN2}$, $\overline{CSR}$ can be mapped independently.

RAM's can be enabled in 1K blocks through jumper straps (See FIG 4)

For 1K of on board RAM: Place E53 to E54,
For 2K of on board RAM: Place E53 to E54, E51 to E52
For 3K of on board RAM: Place E53 to E54, E49 to E50, E51 to E52
For 4K of on board RAM: Place E47 to E48, E49 to E50, E51 to E52, E53 to E54

NOTE: $\overline{EN2}$ is functional when 2732 (4K x 8) EPROM's are used, otherwise it has to be pulled high.

9.2 Power On/Push-Button Reset Restart (Fig 5)

9.2.1 The card has the capability to jump on power on or at any time when the push button reset is pressed to a preassigned location where it is initially programmed. This option can be disabled or enabled through the appropriate jumper straps.

9.2.1 To disable the option:

Place: E9 to E8
E6 to E7
Select the desired memory blocks by jumpering them to the appropriate starting addresses.

Remove: E9 from E10

9.2.2 To start the CPU at any location within the address field other than 0000H and within on board memory range.

Place: E9 to E10
E6 to E7
Map the desired memory blocks by jumpering them to their subsequent starting addresses (EN1 should be strapped to where the power on jump should go) the on board RAM can also be mapped to start at 0000H by jumpering
E5 to E4

Remove: E8 to E10
E8 to E7

Place the following instruction codes at the first 3 bytes of EPROM located at 4F.

C3 03 ( )
└── Power on Starting Address

9.2.3 To start the CPU on power On, other than 0000H at the address not within on board memory range, but placed on another module within the STD Microcomputer System:

Place: E8 to E7
E9 to E10
Map the desired memory block by strapping them to their subsequent starting addresses (Note: EN1 should be strapped to where the power on jump should go).

Place the following instruction codes at the first 3 bytes of EPROM located at 4F.

C3 03 ( )

Power on starting address

Remove E6 to E7
E8 to E10

9.3 EPROM 2716 (2K x 8) or 2732 (4K x 8) Selection (FIG: 6)
Either 2716 or 2732 can be selected by appropriate jumper straps.

To select 2716:

Place E30 to E31
E29 to E28
E11 to E12
Strap Pin 21 of EPROM's to VCC

Remove E30 to E31
E29 to E28

To Select 2732:

Place E32 to E31
E27 to E28
Strap Pin 21 of EPROM's to ADD11

Remove E12 from E11
E30 to E31
E29 to E28

9.4 $\overline{\text{MEMEX}}$, $\overline{\text{IOEXP}}$ See Fig 7

$\overline{\text{MEMEX}}$ or $\overline{\text{IOEXP}}$ can be jumpered to ground (E33) to enable off board memory and I/O all the time; or it can be pulled high through E36 to disable any off board I/O or memory operation. They can also be strapped to E37 (STD Bus Buffer enable), to ensure during any on board I/O or memory operation, the external I/O or memories are disabled.

9.5 Internal/External Clock Selection

External or internal clocks can be disabled or enabled through appropriate jumpers shown in FIG. 8 and 9 for Z80 Processor of each timer/counter clock/trigger input.

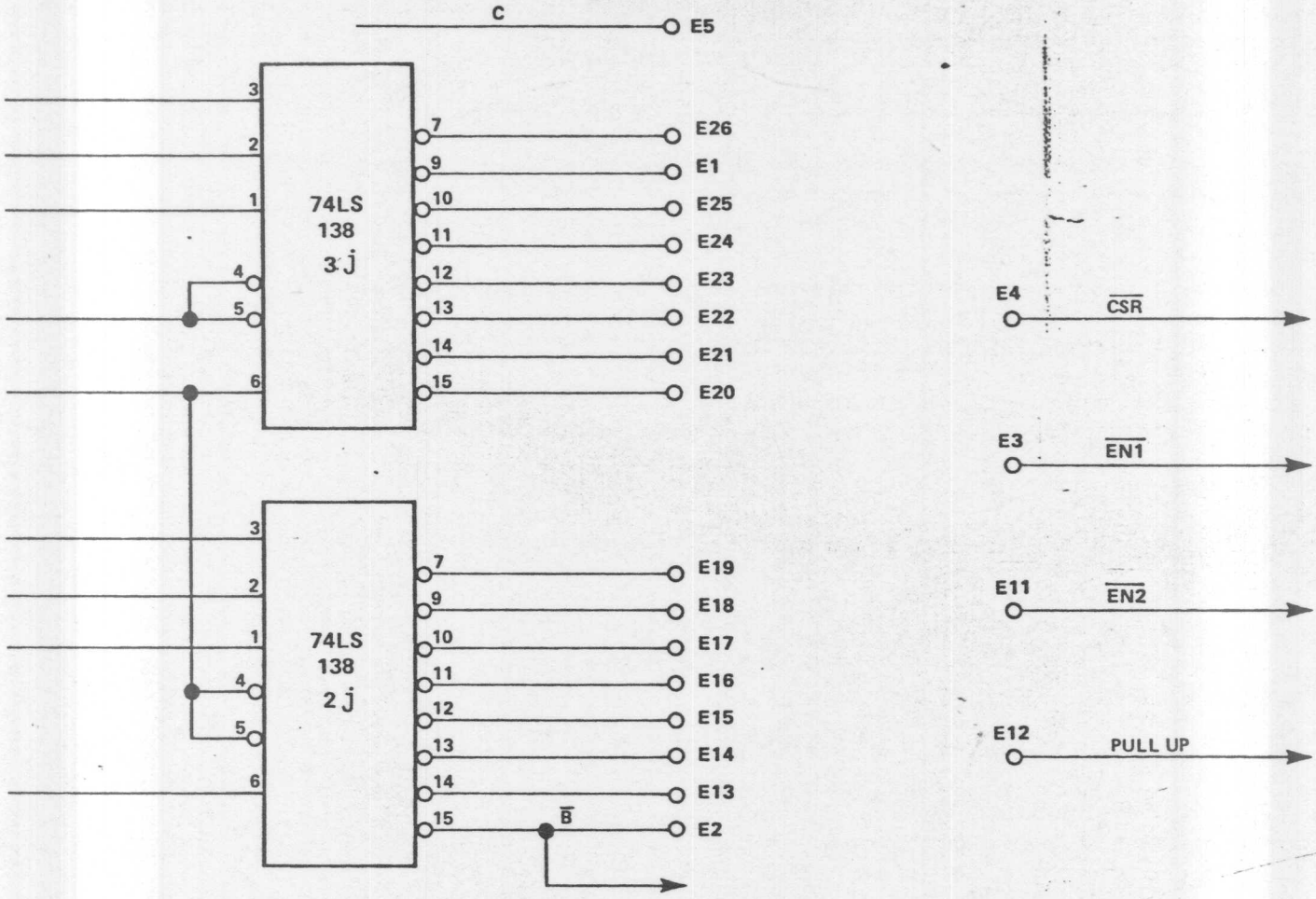

C
E5
3
2
1
4
5
6
74LS
138
3 j
7
9
10
11
12
13
14
15
E26
E1
E25
E24
E23
E22
E21
E20
E4
CSR
E3
EN1
74LS
138
2 j
E19
E18
E17
E16
E15
E14
E13
E2
B
E11
EN2
E12
PULL UP

FIG: 3

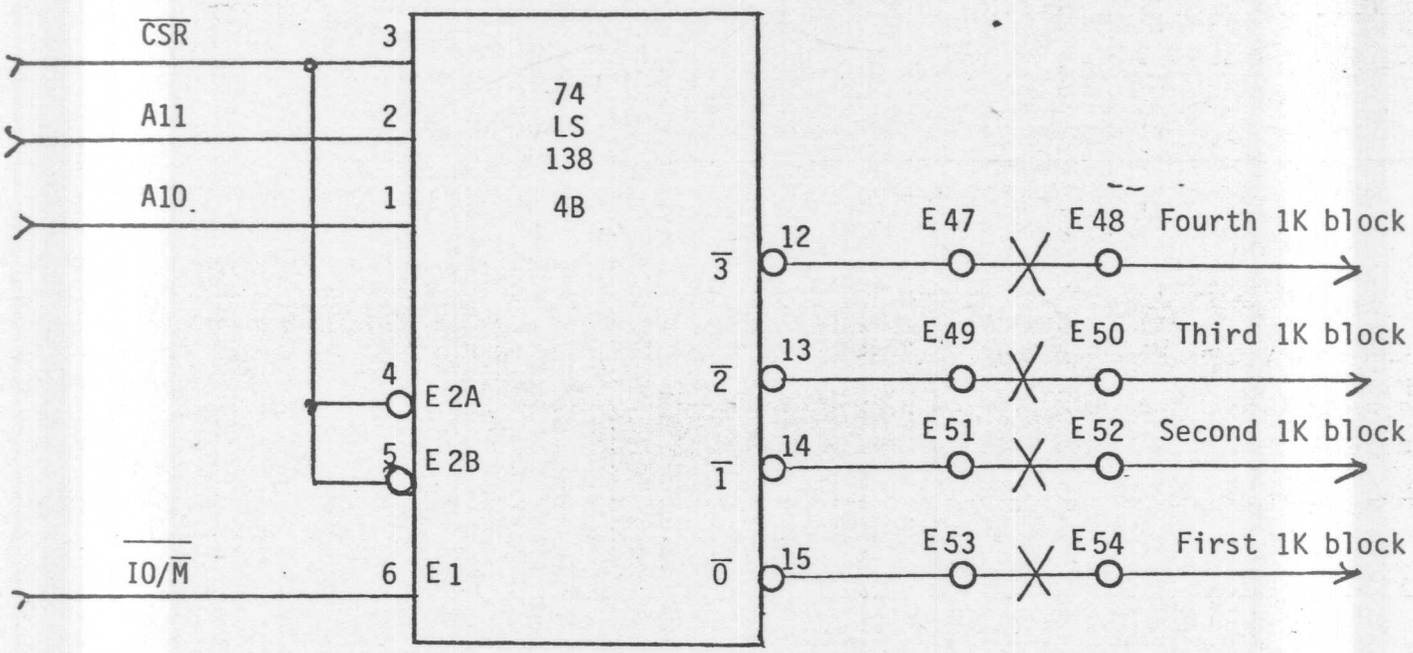


FIG: 4

Designate the printed circuit trace

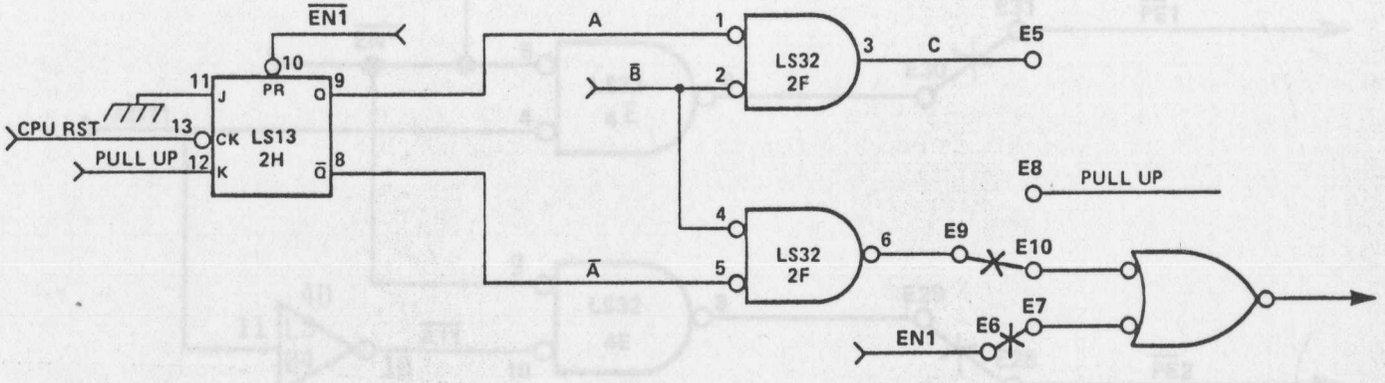


FIG: 5

Designate the printed circuit trace.

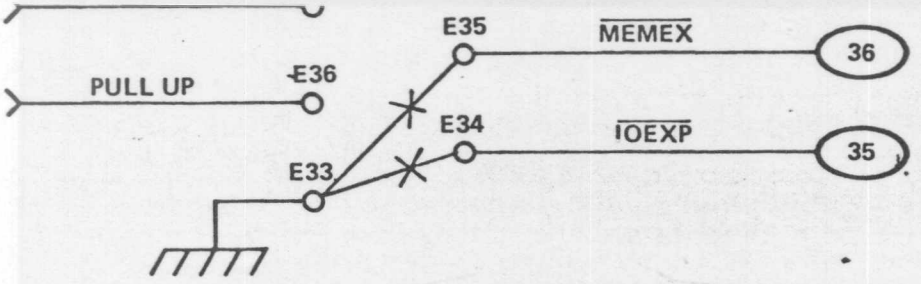


FIG 7

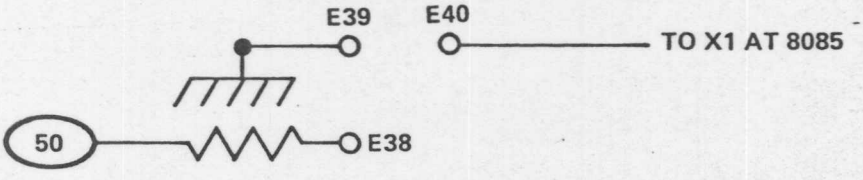


FIG: 8

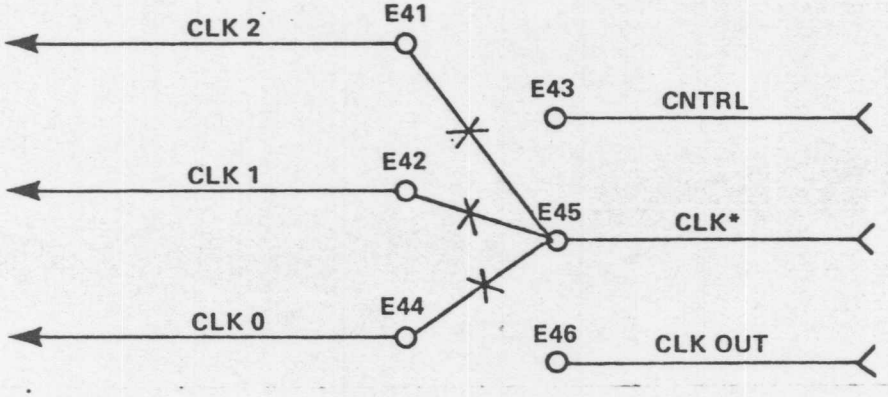


FIG: 9

10.0 CARD DC CHARACTERISTICS

PARAMETER	LIMITS
Power V_{CC}	5V ±5% at 1.5A Max.
Operating Temperature	0 to 55°C
Input Loading	1 LS* Max.
Output Drive	60 LS* Loads Max.
Output 3-State Leakage	1 LS* Loads Max.

*Low-power Schottky

SYMBOL	PARAMETER	CLOCK FREQUENCY			
		3.0 MHz		4.0 MHz	
		MIN. (ns)	MAX. (ns)	MIN. (ns)	MAX. (ns)
t_{CYC}	CLK Cycle Period	325.0		250.0	
t_1	CLK Low Time	102.5		65.0	
t_2	CLK High Time	132.5		95.0	
$t_{r,f}$	CLK Rise and Fall Time		30.0		30.0
t_{AC}	A0-15 Valid to Leading Edge of Control	210.0	135.0		
t_{AD}	Address Valid to Valid Data In		612.5		425.0
t_{AL}	Address Valid before Trailing Edge of SYNC	82.5		45.0	
t_{ARY}	WAIT Valid from Address Valid		260.0		150.0
t_{AC}	Address Valid after Control	122.5		85.0	
t_{CC}	Width or Control Low (RD, WR, INTA) Edge of SYNC	417.5		305.0	
t_{CL}	Trailing Edge of Control to Leading Edge of SYNC	87.5		50.0	
t_{DW}	Data Valid to Trailing Edge of WRITE	417.5		305.0	
t_{HABE}	BUSAK to Bus Enable		212.5		175.0
t_{HABF}	Bus Float after BUSAK		212.5		175.0
t_{HACK}	BUSAK Valid to Trailing Edge of CLK	102.5		65.0	
t_{HDH}	BUSRQ Hold Time	0	0	0	0
t_{HDS}	BUSRQ Setup Time to Trailing Edge of CLK	150.0		100.0	
t_{INH}	INTR Hold Time	0	0	0	0
t_{INS}	INTR, Setup Time to Failing Edge of CLK	140.0		130.0	
t_{LC}	Trailing Edge of SYNC to Leading Edge of Control	122.5		85.0	
t_{LCK}	SYNC High During CLK Low	112.5		75.0	
t_{LDR}	SYNC to Valid Data During Read		600.0		450.0
t_{LOW}	SYNC to Valid Data During Write		200.0		150.0
t_{LL}	SYNC Width	142.5		105.0	
t_{LRY}	SYNC to WAIT Stable		90.0		30.0
t_{RAE}	Trailing Edge of READ to Re-Enabling of Address	152.5		115.0	
t_{RD}	READ (on INTA) to Valid Data		317.5		205.0
t_{RV}	Control Trailing Edge of Leading Edge of Next Control	407.5		295.0	
t_{RDH}	Data Hold Time after Read INTA	0	0	0	0
t_{RYH}	WAIT Hold Time	0	0	0	0
t_{RYS}	WAIT Setup Time to Leading Edge of CLK	90.0		80.0	
t_{WD}	Data Valid after Trailing Edge of WRITE	122.5		85.0	
t_{WDL}	Leading Edge of WRITE to Data Valid		40.0		20.0

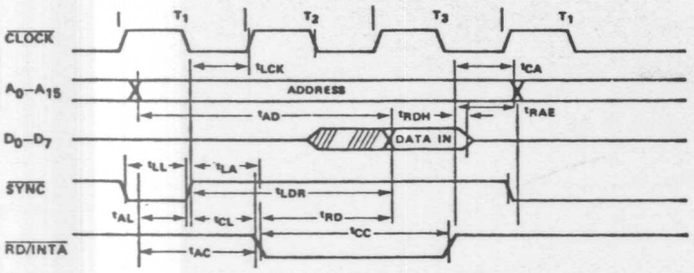
Note: To calculate timing specifications when wait state(s) are present, use the following equations:

$t_{AD} = \left(\frac{5}{2} + N\right) T - 150$ max.

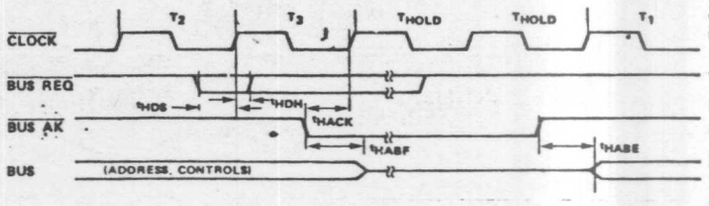
$t_{RD} = \left(\frac{3}{2} + N\right) T - 150$ max.

$t_{DW} = \left(\frac{3}{2} + N\right) T - 70$ min.

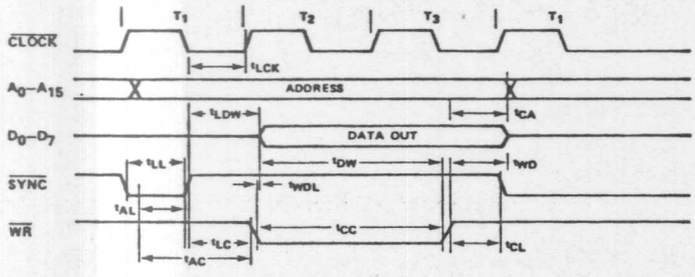
$t_{CC} = \left(\frac{3}{2} + N\right) T - 70$ min.



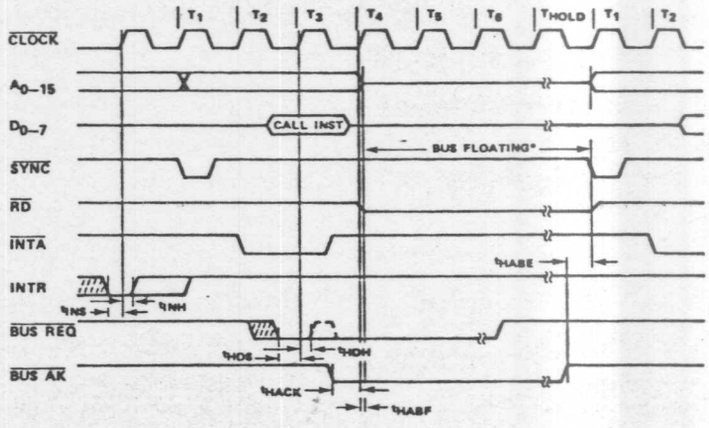
READ OPERATION



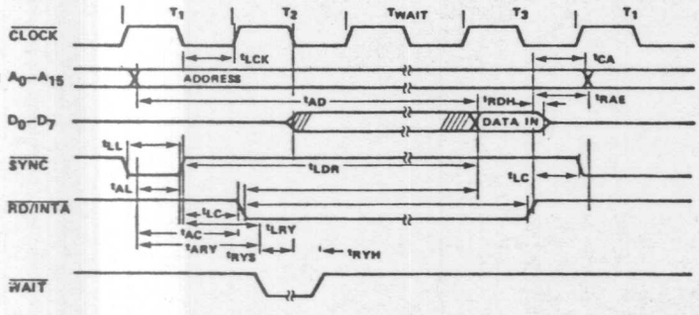
BUS REQUEST OPERATION



WRITE OPERATION



INTERRUPT AND BUS REQUEST



READ OPERATION with WAIT CYCLE (Typical)
(same READY timing applies to WRITE operation)

12.0 ORDERING INFORMATION:

PART NO.	CLOCK FREQ.	DESCRIPTION
ISB-3110-01	4.0 MHz	4K Bytes of RAM strapped to start at 1000_H
ISB-3110-08	3.0 MHz	Two EPROM sockets strapped to start at 0000_H
ISB-3110-02	4.0 MHz	No internal RAM, one EPROM supplied with first 3 bytes programmed to power-on start the CPU at location $E000_H$
ISB-3110-09	3.0 MHz	
ISB-3110-03	4.0 MHz	One EPROM with first 3 Bytes programmed to power-on start the CPU at $E000_H$. 2K bytes of RAM mapped at $E800_H$.
ISB-3110-10	3.0 MHz	
ISB-3110-04	4.0 MHz	3K Bytes of RAM starting at 1000_H
ISB-3110-11	3.0 MHz	2 EPROM sockets starting at 0000_H
ISB-3110-05	4.0 MHz	2K Bytes of RAM starting at 1000_H
ISB-3110-12	3.0 MHz	2 EPROM sockets starting at 0000_H
ISB-3110-06	4.0 MHz	1K Bytes of RAM starting at 1000_H
ISB-3110-13	3.0 MHz	2 EPROM sockets starting at 0000_H
ISB-3110-07	4.0 MHz	No RAMs
ISB-3110-14	3.0 MHz	2 EPROM sockets starting at 0000_H

Word Size: 8-Bit Data Bus
Instruction: 8, 16, 24 Bits

Clock Period (T State):

NOTE:

Two EPROM sockets are provided. The EPROM's with appropriate ODT or other kind of executive or utility programs can be ordered separately.